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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,307	07/01/2003	Akihiro Matsuda	10873.352USRE	3972
53148	7590	10/24/2006	EXAMINER	
HAMRE, SCHUMANN, MUELLER & LARSON P.C. P.O. BOX 2902-0902 MINNEAPOLIS, MN 55402			DICKEY, THOMAS L	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 10/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/611,307

Applicant(s)

MATSUDA ET AL.

Examiner

Thomas L. Dickey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 April 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 July 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 09/209,214.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>08/28/2003</u> . | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. The preliminary amendment filed on 07/06/98 has been entered.

Information Disclosure Statement

2. The Information Disclosure Statement filed on August 2, 1996 has been considered.

Reissue Applications

3. Claims 1-14 are rejected under 35 U.S.C. 251 as being based upon a defective reissue declaration. See 37 CFR 1.175.

A. The reissue oath/declaration filed with this application is defective because it fails to identify at least one error that is relied upon to support the reissue application. See 37 CFR 1.175(a)(1) and MPEP § 1414.

B. Claims 6-14 are rejected under 35 U.S.C. 251 as being an improper recapture of broadened claimed subject matter surrendered in the application for the patent upon which the present reissue is based. See *Pannu v. Storz Instruments Inc.*, 258 F.3d 1366, 59 USPQ2d 1597 (Fed. Cir. 2001); *Hester Industries, Inc. v. Stein, Inc.*, 142 F.3d 1472, 46 USPQ2d 1641 (Fed. Cir. 1998); *In re Clement*, 131 F.3d 1464, 45 USPQ2d 1161 (Fed. Cir. 1997); *Ball Corp. v. United States*, 729 F.2d 1429, 1436, 221 USPQ 289, 295 (Fed. Cir. 1984). A broadening aspect is present in the reissue that was not present in the application for patent. The record of the application for the patent shows

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that the broadening aspect (in the reissue) relates to claim subject matter that applicant previously surrendered during the prosecution of the application. Accordingly, the narrow scope of the claims in the patent was not an error within the meaning of 35 U.S.C. 251, and the broader scope of claim subject matter surrendered in the application for the patent cannot be recaptured by the filing of the present reissue application.

Claim 1 of parent 09/209,214 originally recited (as does claim 6 of the instant reissue application) a semiconductor device including substrate, semiconductor element including first dielectric layer, dummy semiconductor element, and spacing between semiconductor element and dummy semiconductor element. Both Takaishi 5,689,126 and Uehara et al. 5,946,563 anticipated claim 1 of '214. Claim 4 of '214 added to claim 1 the limitation that the first dielectric layer be composed of a material selected from a dielectric material having a dielectric constant of 100 or more and a ferroelectric material. Only Takaishi anticipated claim 4. Claim 7 of '214 added to claim 1 the limitation that the semiconductor device be a transistor in which the electrode works as a gate electrode of the transistor. Only Uehara et al. anticipated claim 7.

On 05/24/2001, recognizing that Takaishi anticipated claim 4, Applicants cancelled claim 4. Applicants amended claim 1 to combine the limitations of claims 1, 4, and 7. The new claim 1 combination of original claims 1, 4 and 7 avoided Uehara et al. (as original claim 4 had). Further, the new claim 1 combination of original claims 1, 4 and 7

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avoided Takaishi (as original claim 7 had). On this basis the '214 application passed to issue and became 6,320,214.

Claim 6 of the present reissue application recites a combination that differs from the patented combination in that it does not include the critical "transistor in which the electrode works as a gate electrode" limitation, instead adding a limitation (the method recited in aid of understanding the exact nature of the claimed multilayer) not previously examined or argued. However, the added limitation does not prevent the original application's claim 4 (said claim having been surrendered during prosecution of the patent) from reading onto presently presented claim 6.

Applicants may argue that because present claim 6 is different from original claim 4, present claim 6 was not surrendered. However, such an argument would ignore the key fact that cancelled claim 4 of the original application reads on present claim 6. When Applicant surrendered original claim 4, Applicant surrendered all subject matter that original claim 4 reads on.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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Claims 6,8,11, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by TAKAISHI (5,689,126).

Takaishi discloses a semiconductor device comprising a semiconductor device, being a capacitor element, comprising a substrate 1, a multilayer 15 formed on the substrate 1, the multilayer comprising a semiconductor element on the substrate 1, the semiconductor element including a first dielectric layer 12 (the first dielectric layer 12 being composed of a material (BST or PZT, note column 5 line 19) selected from a dielectric material having a dielectric constant of 100 or more and a ferroelectric material) an electrode 13 on the first dielectric layer 12, and a bottom electrode 11 between the first dielectric layer 12 and the substrate 1; and a dummy semiconductor element (dummy capacitor) on the substrate 1, the dummy semiconductor element including a second dielectric layer 12' a dummy electrode 13' on the second dielectric layer 12', and a dummy bottom electrode 11' between the second dielectric layer 12' and the substrate 1 wherein the dummy semiconductor element is located so that a space between the electrode 13 and the dummy electrode 13' is in a predetermined range. Note figures 6,7, column 4 lines 58-66, and column 5 lines 1-32 of Takaishi.

The applicant's claims 6,8,11, and 14 do not distinguish over the Takaishi reference regardless of the process used to form the multilayer, electrode, dummy electrode, first dielectric layer, second dielectric layer bottom electrode, and dummy bottom electrode, because only the final product is relevant, not the recited process of forming a dielectric

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film for the first dielectric layer and the second dielectric layer; forming an electrically conductive film on the dielectric film; and etching the electrically conductive film so as to form the electrode and the dummy electrode, etching the dielectric film so as to form the first dielectric layer and the second dielectric layer, and forming (optional) a bottom electrically conductive film for the bottom electrode and the dummy bottom electrode between the dielectric film and the substrate by etching the bottom electrically conductive film so as to form the bottom electrode and the dummy bottom electrode. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006) (“While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.”)

Note that when “product by process” claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims

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or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

The Federal Circuit recently revisited the question of whether a “product by process” claim can be anticipated by a reference that does not recite said process. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d at 1099-1101. The Federal Circuit cited with approval this Office's current statement of the law, found in MPEP § 2113:

[Even] though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.

Id. at 1101. The Federal Circuit held this statement to be consistent with its own views on this topic, as well as various Supreme Court rulings, notably *Gen. Elec. Co. v. Wabash Appliance Corp.*, 304 U.S. 364, 373 (1938) (“Although in some instances a claim may validly describe a new product with some reference to the method of production, a patentee who does not distinguish his product from what is old except by reference, express or constructive, to the process by which he produced it, cannot secure a monopoly on the product by whatever means produced.”). *Id.*

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

A. Claims 1,2,5-10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over TSUCHIYA (JP57180182A) in view of UEHARA ET AL. (5,946,563).

Tsuchiya discloses a semiconductor device comprising a substrate 1, a semiconductor element 6-9 on the substrate 1, the semiconductor element 6-9 including a first dielectric layer 9 (the first dielectric layer 9 being composed of a material selected from a dielectric material having a dielectric constant of 100 or more and a ferroelectric material) and an electrode 6 on the first dielectric layer 9; wherein the semiconductor device is a transistor (indicated by source 2 and drain 3) in which the electrode 6 works as a gate electrode 6 of the transistor and a multilayer 6-7-8-9 is formed on the substrate 1, the multilayer comprising the semiconductor element 6-9. Note figure 1 and the English language Abstract of Tsuchiya. Tsuchiya does not disclose a dummy semiconductor element 6-9 on the substrate 1, the dummy semiconductor element 6-9 including a second dielectric layer and a dummy electrode 6 on the second dielectric layer, wherein the dummy semiconductor element 6-9 is located so that a space between the electrode 6 and the dummy electrode 6 is in a predetermined range at a spacing of .3 to 5, 9 or 14 microns.

However, Uehara et al. discloses a semiconductor device having gate electrode 50a and dummy semiconductor element 19b-50b-21a on the substrate, the dummy

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semiconductor element including a second dielectric layer 21a and a dummy electrode 50b on the second dielectric layer 21a, wherein the dummy semiconductor element located so that a space S (note column 10 line 56) between the electrode and the dummy electrode 50b is in a predetermined range. With regard to claims 2,5,9,7,12, and 13 Uehara et al. discloses that dummy electrode 50b surrounds electrode at a spacing of .4 microns. Note figure 1b, column 9 lines 47-67, and column 10 lines 1-57 of Uehara et al. Uehara et al. explain, see abstract, that the dummy electrodes allow the real gate electrodes to be miniaturized in a uniform fashion, allowing high integration and higher speed operation. Therefore, it would have been obvious to a person having skill in the art to augment Tsuchiya's semiconductor device with the dummy electrodes such as taught by Uehara et al. in order to allow the real gate electrodes to be miniaturized in a uniform fashion to thus allow high integration and higher speed operation.

The applicant's claims 1,6,10,2,7,12,13,5,8, and 9 do not distinguish over the Tsuchiya and Uehara et al. references regardless of the process used to form the multilayer, electrode, dummy electrode, first dielectric layer, second dielectric layer bottom electrode, and dummy bottom electrode, because only the final product is relevant, not the recited process of forming a dielectric film for the first dielectric layer and the second dielectric layer; forming an electrically conductive film on the dielectric film; and etching the electrically conductive film so as to form the electrode and the dummy electrode, etching the dielectric film so as to form the first dielectric layer and

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the second dielectric layer. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006) (“While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.”)

Note that when “product by process” claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

The Federal Circuit recently revisited the question of whether a “product by process” claim can be anticipated by a reference that does not recite said process. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d at 1099-1101. The Federal Circuit cited with approval this Office’s current statement of the law, found in MPEP § 2113:

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Id. at 1101. The Federal Circuit held this statement to be consistent with its own views on this topic, as well as various Supreme Court rulings, notably *Gen. Elec. Co. v. Wabash Appliance Corp.*, 304 U.S. 364, 373 (1938) ("Although in some instances a claim may validly describe a new product with some reference to the method of production, a patentee who does not distinguish his product from what is old except by reference, express or constructive, to the process by which he produced it, cannot secure a monopoly on the product by whatever means produced."). Id.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

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information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'T. L. Dickey', with a large, stylized initial 'T' and 'D'.

Thomas L. Dickey
Primary Examiner
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